WHAT IS CLAIMED IS:

1. A real time embedded video processing system, comprising:

a real time operating system;

a graphics application that generates computer graphics in response to user input;

an input control application that controls at least one of video input source in response to user input; and

a video processing engine that receives input from at least one of the video input sources and receives computer graphics from the graphics application, the video processing engine blending the computer graphics with the input and outputting the blended data in substantially real time.

2. The system of claim 1, further comprising an input/output (I/O) interface that communicates with a user input device.

3. The system of claim 2, in which the I/O interface communicates with a mass storage device.

4. The system of claim 3, in which the video processing engine receives input from the mass storage device and overlays the computer graphics on the input received from the mass storage device in real time.

5. The system of claim 2, in which the I/O interface is a USB interface.

6. The system of claim 1, in which the video processing engine comprises a dedicated logic circuit, at least one encoder, at least one video decoder, and a video buffer.

7. The system of claim 6, in which the dedicated logic circuit comprises a field programmable gate array (FPGA)

8. The system of claim 1, in which the plurality of video input sources have a plurality of different control protocols.

9. The system of claim 8, in which the protocols comprise at least one of RS-232, RS-422, Control-M, LANC, and infrared.

10. The system of claim 1, in which the plurality of video input sources generate video streams having a plurality of different formats.

11. The system of claim 10, in which the different formats comprise at least one of YUV, RGB, S-Video, composite, VGA, and DVI.

12. The system of claim 11, in which the system translates video from one of the formats to another of the formats.

13. The system of claim 10, in which one of the video streams is in a YUV format, and the video processing engine digitally color maps the YUV format into an RGB format.

14. The system of claim 1, in which the video processing engine outputs the blended data to a plurality of output devices.

15. The system of claim 1, in which the user input device comprises a PDA comprising a client application that communicates with a host application within the system.

16. The system of claim 1, in which the blended data is stored as an image file.

17. The system of claim 1, in which the system is portable.

18. A dedicated logic circuit for real time video processing, comprising:

a pixel processing engine that receives input from a video input source and receives computer graphics from a graphics application, the pixel processing engine alpha blending the computer graphics with the video input source and outputting the blended data in substantially real time.

19. The dedicated logic circuit of claim 18, further comprising a buffer controller that controls an external buffer, and a CPU interface that receives the computer graphics..

20. The dedicated logic circuit of claim 18, in which the dedicated logic circuit processes a plurality of input video streams and outputs a plurality of output video streams, the streams having a plurality of different formats.

21. A real time embedded video processing system, comprising:

a central processing unit (CPU);

a real time operating system that communicates with the CPU;

an input/output (I/O) interface that receives user input via a wireless user input device;

a graphics application that generates computer graphics in response to user input received from the user input device, the application interfacing with the CPU via the operating system;

a device remote control application that controls a plurality of different video input devices in response to user input received from the user input device; and

a video processing engine comprising a field programmable gate array (FPGA), a video buffer, at least one video decoder, and at least one video encoder, the FPGA comprising a CPU interface, a video buffer controller, and a pixel processing engine that receives input from at least one of the video input sources via at least one of the video decoders and receives computer graphics from the graphics application via the CPU and the CPU interface, the pixel processing engine alpha blending the computer graphics with the input and outputting the blended data in real time to at least one of the video encoders.

22. The system of claim 20, in which the system is portable.